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DIGITAL CLOCK RECOVERY CIRCUIT EMPLOYING FIXED CLOCK OSCILLATOR DRIVING FRACTIONAL DELAY LINE

ABSTRACT

A clock recovery scheme for a digital communication receiver has a fixed fractional delay line that is driven by a fixed frequency reference clock source, to provide a plurality of respectively offset phase delayed versions of the reference clock. A phase lock loop, to which the received signal is coupled, controllably steps through the phase delayed versions of the reference clock, so as to controllably increase or decrease the effective frequency of the reference clock and thereby produce a recovered clock signal.